In the Specification:

Please amend paragraph [0006] as follows:

FIGS. 4A-C show plan view representations of recordings taken by a scanning electron microscope, abbreviated to SEM ~~hereinafter,~~ hereinafter. The plan view recordings are of trenches of storage capacitances in different depths of a semiconductor substrate, [[said]] and the trenches are ~~being~~ arranged in checkered fashion in alternation with unpatterned fields. The recordings each show an arrangement of structures which are based on a rectangular pattern in a mask layout and are transferred and etched into a semiconductor substrate in a conventional manner.

Please amend paragraph [0013] as follows:

The invention provides for a method for increasing a structure size of main structures such as trenches--formed in essential parts deep within ~~in a depth of~~ a semiconductor substrate--by means of an etching process which expands the main structures in the depth of the semiconductor ~~substrate, provision being made of the~~ substrate. The semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that define a sidewall of a main structure, such as a trench structure for example that are more resistant to etching and with crystal faces that define other sidewalls of the main structure that are less resistant to etching, and the main structures being arranged in checkered fashion in first areas of a rectangular surface grid, at a surface of the semiconductor ~~substrate, in each case in alternation with~~ substrate. Each of the first areas alternate with second areas for forming secondary structures formed ~~in each case~~ essentially in a section of the semiconductor substrate that is near the surface.

Please amend paragraph [0018] as follows:

FIGS. 4A-C show SEM plan view recordings of trenches in a semiconductor wafer [[in]] at different depths,

Please amend paragraph [0019] as follows:

FIGS. 5A-D show SEM plan view recordings of structures according to the invention [[in]] at semiconductor wafer in different depths,

Please amend paragraph [0021] as follows:

FIGS. 7A-B respectively show diagrammatic plan views of surfaces of a semiconductor substrate processed conventionally and of a semiconductor substrate processed according to the invention, and

Please amend paragraph [0024] as follows:

For the method according to the invention, a mask 3 and a semiconductor wafer 1 made of monocrystalline silicon are arranged in the manner shown in FIG. 1. The semiconductor wafer 1 is provided with a marking 2 according to the invention, which marking is rotated by 45 degrees with respect to conventionally marked semiconductor wafers and identifies the <100> crystal orientation of the silicon. By means of the marking, the mask 3 is oriented to the crystal orientation in the semiconductor wafer. The mask structure is thus imaged along a different crystal orientation compared with conventional methods.

Please amend paragraph [0026] as follows:

FIG. 3 shows a structure which is etched into a semiconductor substrate 6 and is designed as a trench 4. ~~On account~~ As a result of a further etching step below a selected trench depth of about one micrometer, the trench has a bottle-like expansion or extension 5 for enlarging [[an]] the electrode area of a storage capacitance to be formed in ~~processed from~~ the trench. The upper section of the trench 8 is provided with a protective layer which prevents lateral etching into the semiconductor substrate 6 in regions near the surface.

Please amend paragraph [0028] as follows:

FIG. 4A illustrates the upper parts--provided with a protective layer--of the trenches 8, the sidewalls of ~~which~~ the upper parts form an oval ~~and the~~ having a long side ~~of which is~~ arranged parallel to the <110> crystal orientation. Such a [[side]] sidewall is called <110> sidewall 7 for short hereinafter.

Please amend paragraph [0029] as follows:

Deeper in the semiconductor substrate, approximately where the protective layer ends, is the cross section of the trench illustrated in FIG. 4B ~~results~~, said cross section showing a bottle-like expanded area or extension 5. And as shown, below ~~Below~~ the protective layer, the sidewalls [[form]] have a rectangle shape with <110> sidewalls 7. Intermediate walls formed from the semiconductor substrate 6 between the sidewalls of the individual trenches 8 have, at their thinnest points, a very small thickness of approximately 20 nanometers, which can lead to short circuits in the case of trenches processed to form storage capacitances, on account of manufacturing tolerances.

Please amend paragraph [0030] as follows:

FIG. 4C represents the bottom 9 of the trenches. The ~~in the region of a~~ trench bottom 9 terminating at the deepest level of the trenches ~~in the depth~~ of the semiconductor substrate. There they have a rectangular form with a smaller cross-sectional area than directly below the protective layer. The sidewalls are [[again]] still <110> sidewalls 7.

Please amend paragraph [0031] as follows:

The trenches shown in FIGS. 5A-D were produced by the method according to the invention. They are based on the same checkered mask layout of FIG. 4. For this purpose, the mask layout is imaged onto a semiconductor wafer oriented according to the invention. ~~Afterward,~~ As was discussed with respect to FIG. 4A, the trenches are etched into the surface of the semiconductor substrate 6 and each trench is again provided with a protective layer that protects against a second etching step in upper sections. FIGS. 5A to 5D illustrate cross sections of the trenches in different depths parallel to the surface 10 of the semiconductor substrate 6.

Please amend paragraph [0032] as follows:

In this case, FIG. 5A shows a plan view of the trenches at the surface 10 of the semiconductor substrate 6. FIG. 5B shows a cross section through the trenches in the region of the protective layer which is below the surface 10. The sidewalls of the upper sections of the trenches in each case form an oval whose long sides are oriented according to the invention parallel to the <100> crystal orientation. Such a side is called <100> sidewall 11 for short hereinafter. FIGS. 5C and 5D represent the cross sections of the trenches below the protective layer 12 in two different depths resulting from the second etching step. The sidewalls of the

trenches form a square with <110> sidewalls 7 in cross section. The sidewalls of the upper section of a trench, which include a protective layer are thus rotated by 45 degrees with respect to the sidewalls of the lower section of the same trench that did not include a protective layer. As can be seen when comparing FIG. 4C with FIG. 5D, the resulting rotated square cross section of the trenches in the region below the protective layer leads to or allows a greater or improved ~~an improved~~ utilization of the area of the semiconductor substrate 6.

Please amend paragraph [0033] as follows:

The improved utilization of area becomes clear from FIGS. 6A-F. The cross sections of the trenches produced according to the invention in FIGS. 6A to 6C were recorded before the etching step (bottle etch)--leading to the bottle-like expansion or extension--in different depths. These expansion areas [[and]] correspond to the smaller cross sections of the prior art trenches in FIGS. 5B to 5C.

Please amend paragraph [0034] as follows:

The cross sections of the trenches after the etching step leading to the bottle-like expansion or extension can be seen on a larger scale in FIGS. 6D to 6F. The cross section--oval in plan view--in the upper section of the trenches with <100> sidewalls 11 is shown in FIG. 6D. FIGS. 6E and 6F show the square cross sections with <110> sidewalls 7 of the bottle-like extensions in two different depths, one above and one below the trench center. The perfect utilization of area in the depth of the semiconductor substrate can clearly be discerned here.

Please amend paragraph [0036] as follows:

A pattern of first areas for the main structure (trench capacitor) and second areas for the secondary (selection transistor) structures 131, 132 is formed on a surface of the semiconductor substrate 6, said pattern being oriented along a surface grid 14. The main and secondary structures 131, 132 are arranged alternately in checkered fashion in the surface grid 14.

Please amend paragraph [0038] as follows:

The secondary structures 132 formed in the second areas are essentially arranged in a section of the semiconductor substrate 6 near the surface between the surface of the semiconductor substrate 6 and a structure edge in the depth of the semiconductor substrate 6. By contrast, substantial parts of the trenches or main structures 131 are formed below the structure edge. The main structures 131 are conventionally expanded below the structure edge by means of a second or bottle etching process. After being expanded by the bottle etching process, the main structures 131 also slightly extend, as illustrated in FIG. 7A, into sections of the semiconductor substrate 6 which lie below the second areas where the secondary structures 132 are formed.

Please amend paragraph [0039] as follows:

In this case, the bottle etching process extends the main structures 131 in a manner independent of direction, so that the maximum possible allowable extension of a main structure 131 is also restricted in the depth of the semiconductor substrate 6 to a field 151 assigned to the main structure 131. Thus, in the prior art method, and is shown in FIG. 7A, sections ~~Sections~~ of the semiconductor substrate which extend below the structure edge under fields 152 assigned to the secondary structures remain unused.

Please amend paragraph [0041] as follows:

~~For this purpose,~~To accomplish this, and as illustrated in FIG. 7B, the surface grid 14 is oriented parallel to crystal faces or sidewalls of the main structures (e.g., trenches) of the semiconductor substrate 6 that are less resistant to etching. In the course of [[an]] etching, crystalline faces having different resistances to etching, hereinafter referred to as area-selective etching ~~process~~, the main structures 131 (e.g., trenches) are formed or extend from the substrate surface into ~~are formed in~~ the depth of the semiconductor substrate 6 below the structure edge with sidewalls that are ideally rotated by 45 degrees with respect to the surface grid 14. [[If]] Therefore, if the rotated main structures 131 are subsequently expanded by means of a bottle etching below the structure edge, then as shown in FIG. 7B, the etching can be substantially increased such that an extended field 161 results for each main structure 131 ~~as maximum extension~~.

Please amend paragraph [0042] as follows:

The semiconductor substrate 6 below the structure edge can be completely assigned to the extended fields 161 and can thus advantageously be utilized almost completely for the expansion or extension of the main structures 131 (such as trenches for capacitors).

Please amend paragraph [0043] as follows:

FIG. 8 illustrates the functional dependence of the number of discharged memory cells AS on the time t.sub.Ret--referred to as "retention time"--for DRAM modules produced from semiconductor wafers processed in rotated fashion according to the invention and from semiconductor wafers processed in nonrotated fashion. Two DRAM modules in each case were

examined for each curve. Curves A and B show the behavior of DRAM modules from semiconductor wafers processed in nonrotated fashion, curve B concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve A. Curves C and D show the behavior in the case of semiconductor wafers processed in rotated fashion according to the invention, curve D again concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve C. The significantly shallower profile of curves C and D compared with curves A and B describes a lengthened "retention time" in the case of semiconductor wafers processed in the rotated fashion of the invention. The influence of the magnitude of the storage capacitance on the "retention time" also becomes clear from curves B and D. A reduced storage capacitance is accompanied by a decrease in the "retention time". In a time interval of 128 ms<t.sub.Ret<8 sec, the following holds true: AS in the case of semiconductor wafers processed in rotated fashion is approximately 0.5* AS in the case of semiconductor wafers processed in nonrotated fashion.

Please amend paragraph [0044] as follows:

Thus, according to the invention, before an etching process which expands the main structure ~~in the depth,~~ deep into the semiconductor wafer, the longitudinal and transverse extents of main structures (e.g., trenches) in the depth of the semiconductor substrate are oriented in rotated fashion with respect to the x, y axes of the surface grid. As a result, the sections of the semiconductor substrate which are located below secondary structures are [[made]] (e.g., the selection transistors) available or useable ~~essentially completely~~ for an extension or expansion of the main structures (e.g., trenches) by means of the etching process to expand ~~which expands~~ the main structure in the depth.

Please amend paragraph [0045] as follows:

As a consequence, significantly larger dimensions and surfaces are possible for the main structures (e.g., trenches) in the deeper levels ~~depth~~ of the semiconductor substrate. If the main structures are formed in each case as electrical trench capacitors ~~capacitances~~ with electrode areas running along the surface, then it is possible to achieve higher capacitance values in comparison with conventional methods given the same space requirement on the surface of the semiconductor substrate by virtue of the better utilization [[of a]] or increased volume available of the semiconductor substrate under the secondary structure. Therefore, given ~~Given~~ identical capacitance values, a large structure having the main and secondary structures can be embodied in a higher density by the method according to the invention.

Please amend paragraph [0046] as follows:

The etching process in the deeper levels of the substrate, which expand ~~expands~~ the main structure in the depth is referred to herein ~~hereinafter~~, for simplification, as bottle etching process. However, such identification is not intended to effect ~~without this effecting~~ a restriction of the [[to]] bottle etching processes ~~in the narrower sense~~.

Please amend paragraph [0047] as follows:

The term secondary structures is also intended to include ~~includes~~ unpatterned sections of the surface of the semiconductor wafer.

Please amend paragraph [0049] as follows:

The longitudinal and transverse extent ~~extents~~ of the main structures [[are]] is oriented in a manner rotated by essentially 45 degrees with respect to the x, y axes of the surface grid to allow the extended use of the substrate at the lower levels. A maximum utilizability of the sections of the semiconductor substrate which are arranged below the secondary structures is therefore possible ~~results in this case~~. Intermediate walls between adjacent main structures are then formed in cross-sectional planes parallel to the surface of the semiconductor substrate with approximately the same thickness.

Please amend paragraph [0050] as follows:

The method according to the invention provides an area-selective etching process. That is, etching crystalline first faces that are less resistant and second faces that are more resistant to an etching process. To that end, provision is made of the semiconductor substrate comprising a crystalline material which has a crystal lattice with crystal faces that can be differentiated. In suitable etching processes, different etching resistances can be derived from the different properties of the crystal faces. The crystal lattice then has crystal faces that are less resistant to etching and crystal faces that are more resistant to etching.

Please amend paragraph [0052] as follows:

Preferably, furthermore, the area-selective etching process is controlled in such a way that, in the deeper levels ~~depth~~ of the semiconductor substrate below a structure edge determined by an extent of the secondary structures ~~into the depth of the semiconductor substrate~~, primary sidewalls of the main structures that are constructed from the crystal faces that are less resistant

to etching are substituted by secondary sidewalls constructed from the crystal faces that are more resistant to etching. The orientation of the crystal faces that are more resistant to etching is rotated in customary semiconductor substrates with respect to the orientation of the crystal faces that are less resistant to etching, so that in this way the orientation--which is intended according to the invention and is rotated with respect to the surface grid--of the longitudinal and transverse extents of the main structure in the depth of the semiconductor substrate is achieved in a particularly advantageous manner.

Please amend paragraph [0057] as follows:

Preferably, in the course of a further processing of the semiconductor substrate, according to one embodiment, the main structures are functionally designed as trench storage capacitances and the secondary structures are essentially designed as selection transistors assigned to the storage capacitances.

Please amend paragraph [0059] as follows:

A mask which prescribes the arrangement at least of main structures (e.g., trenches) is provided with a rectangular pattern for patterning deep trenches each serving as a storage capacitance. The structures on the mask are imaged onto a semiconductor wafer provided with a marking according to the invention, which marking points in the <100> crystal orientation, by means of an exposure device. In this case, the longitudinal side of the imaged rectangles is oriented parallel to the <100> crystal orientation in the semiconductor wafer. The trenches are subsequently etched by means of a dry etching step whose etching speed is dependent on the crystal orientation, in the semiconductor wafer crystal faces with a <100> orientation being

etched more rapidly than crystal faces with a <110> orientation. Only crystal faces with a <110> orientation then remain after a specific etching time. By means of a further etching step, the deep trenches etched in the dry etching step are extended or expanded in bottle-like fashion below a trench depth of about one micrometer. Above one micrometer, the trenches are provided with an etching-resistant protective layer which prevents lateral etching into regions of the semiconductor substrate which are near the surface.

Please amend paragraph [0063] as follows:

After a further etching step having a duration of about 90 seconds, which brings about a bottle-like expansion or extension in the lower section of the trench, the trench in the depth of the semiconductor substrate has a profile that is square in plan view. The thickness of the intermediate walls comprising the semiconductor substrate between the individual trenches is of the order of magnitude of 100 nanometers, instead of about 20 nanometers in the case of semiconductor wafers processed in the prior art nonrotated fashion. It is thus possible to etch significantly larger ~~extensions of the~~ trenches, thereby increasing the electrical capacitance of storage capacitances formed from the trenches. Moreover, the square cross section of the lower part of the trenches leads to an optimum filling of the area of the semiconductor wafer in the depth of the semiconductor substrate.